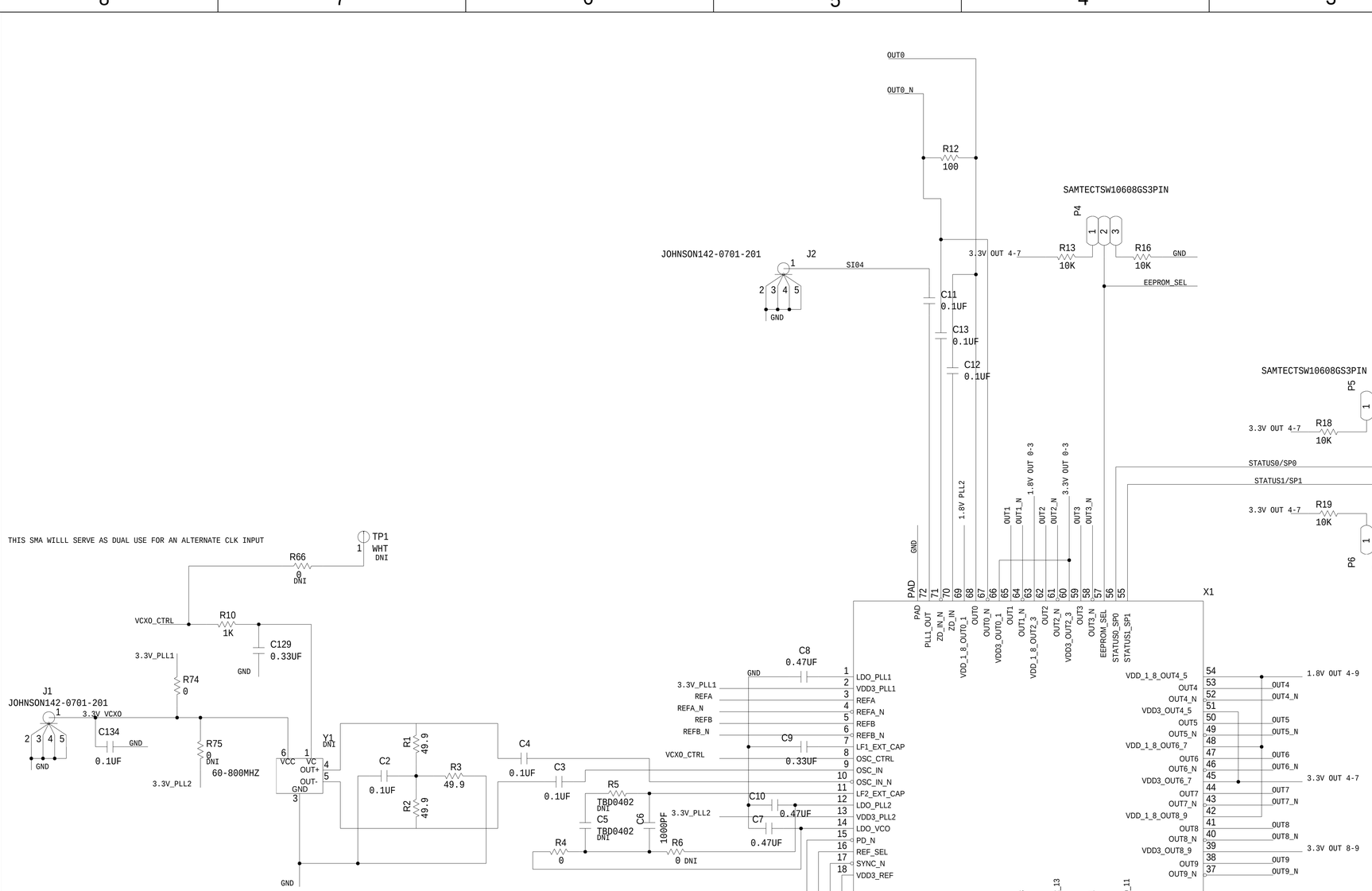
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONFIGURATION FOR CMOS VCXO AND LVPECL VCXO

CMOS VCXO - DNI R1, R2, R3, C2, AND C3. REPLACE C4 WITH 0 OHM RESISTOR.
LVPECL VCXO - R1, R2, R3, C2, C3, C4 AS SHOWN.

CONFIGURATION FOR AD9523 AND AD9523-1

AD9523 - C6 CONNECT TO LDO_VCO PIN 14: R4 = 0 OHM AND R6 = DNI.
AD9523-1 - C6 CONNECT TO LDO_VCO PIN 12: R4 = DNI AND R6 = 0 OHM.

ANALOG DEVICES

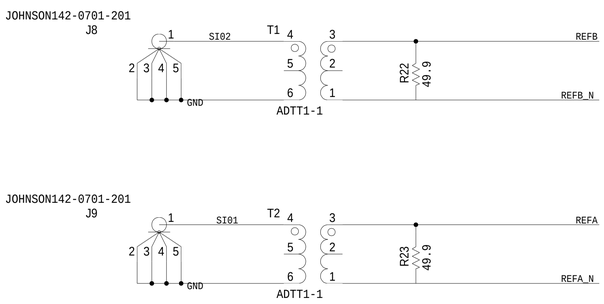
SCHEMATIC

<DRAWING_TITLE_HEADER>
AD9523
EVALUATION BOARD

DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	9523EE01	E
PTD ENGINEER	SIZE / SCALE	SHEET 1 OF 5
R.Huntley	D / NONE	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

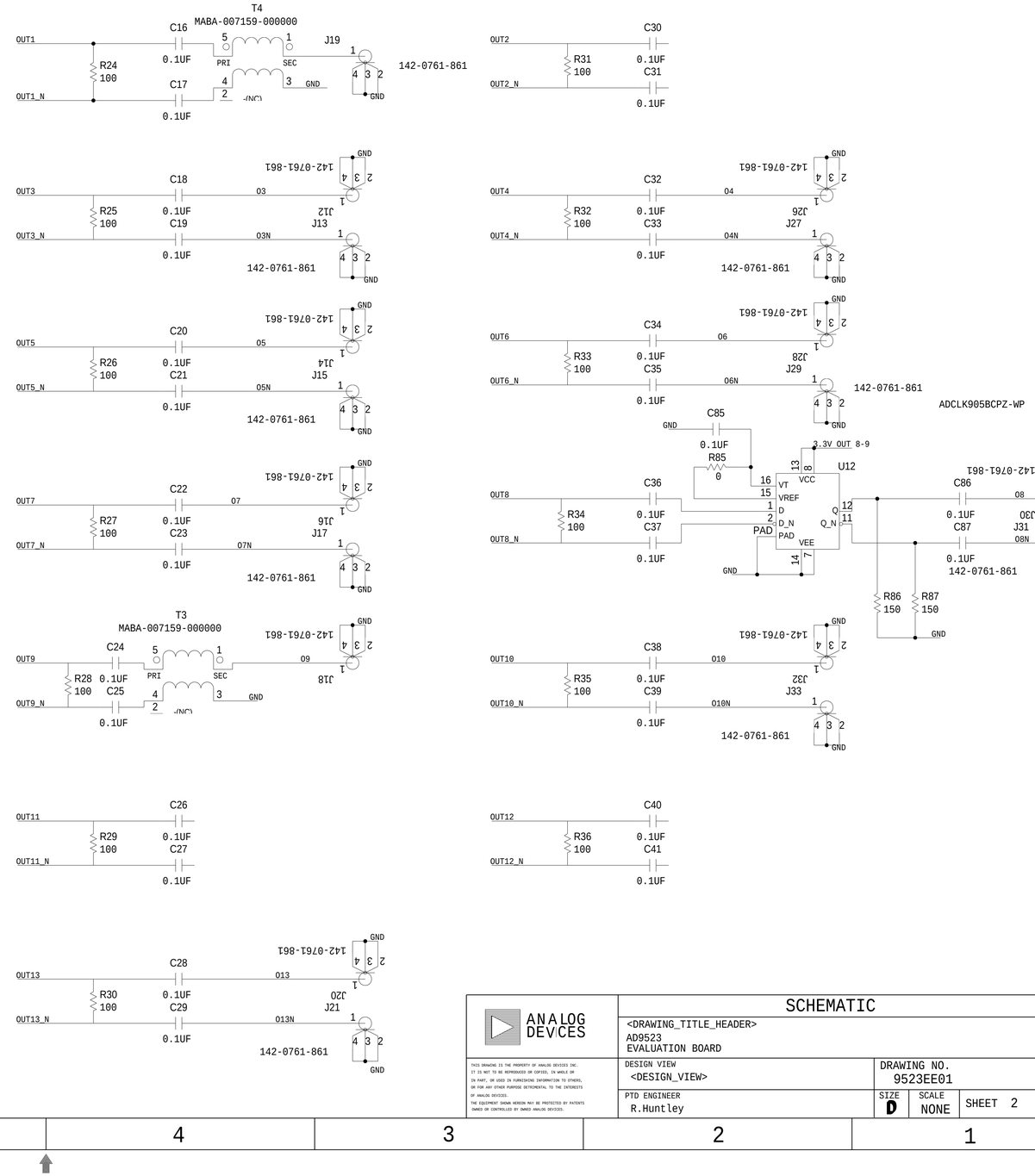
REFERENCE INPUTS



OUTPUT TERMINATIONS

PLACE TERMINATIONS CLOSE TO DUT

ROUTE AS 50OHM SINGLE ENDED TRACES



ANALOG DEVICES

SCHEMATIC

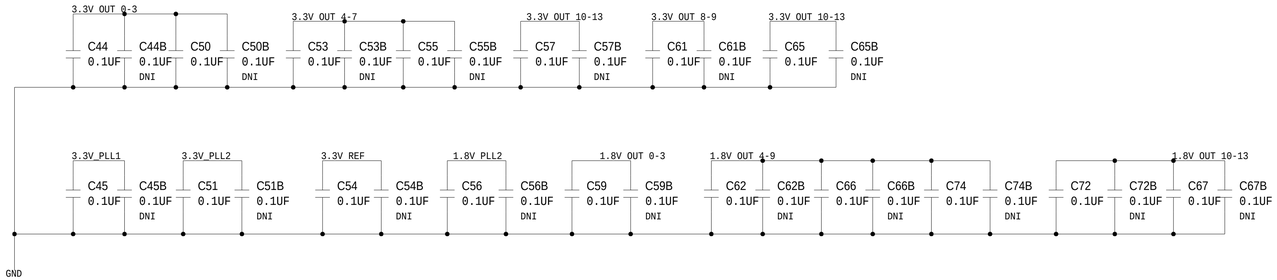
<DRAWING_TITLE_HEADER>
AD9523
EVALUATION BOARD

DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 9523EE01	REV E
PTD ENGINEER R.Huntley	SIZE D / SCALE NONE	SHEET 2 OF 5

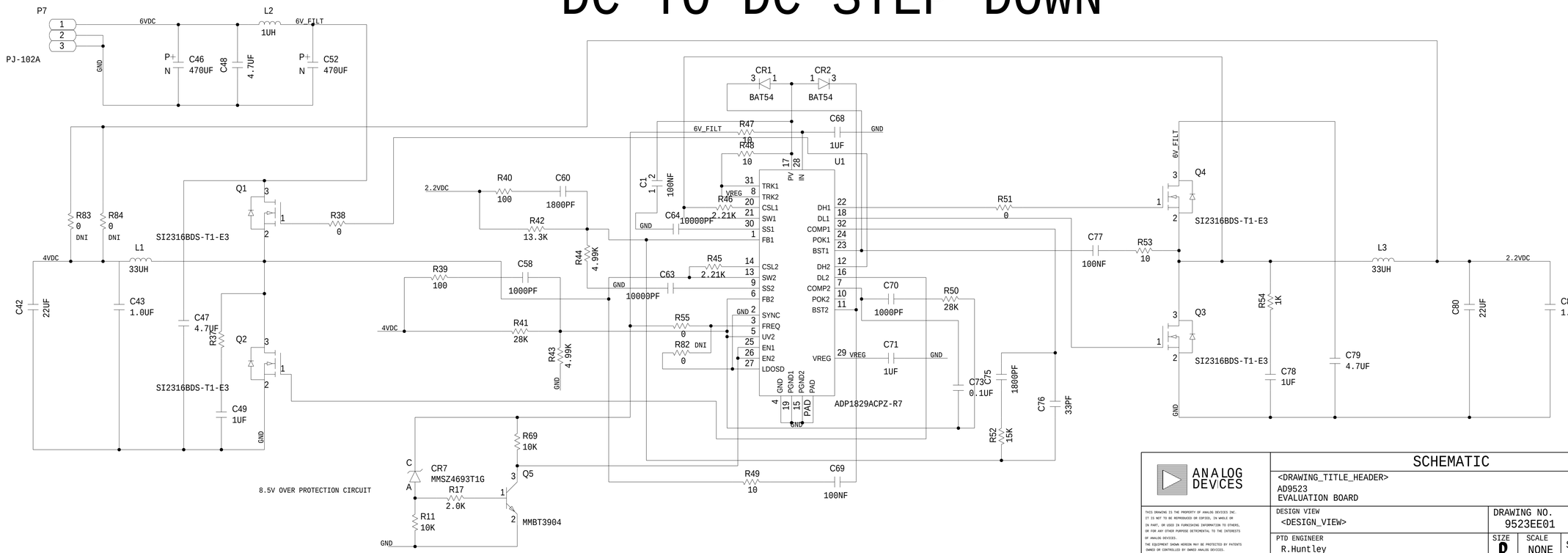
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

BYPASS CAPACITORS

(FOR ONLY THE 9523)



DC TO DC STEP DOWN



ANALOG DEVICES	SCHEMATIC		
	<DRAWING_TITLE_HEADER> AD9523 EVALUATION BOARD		
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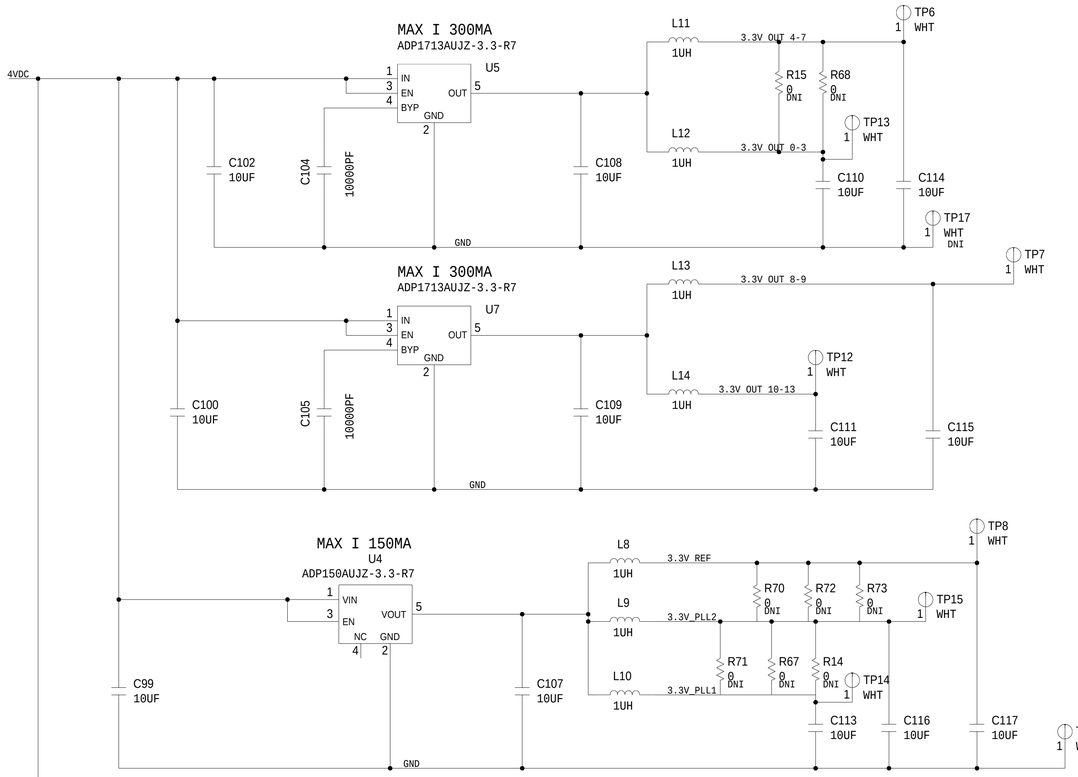
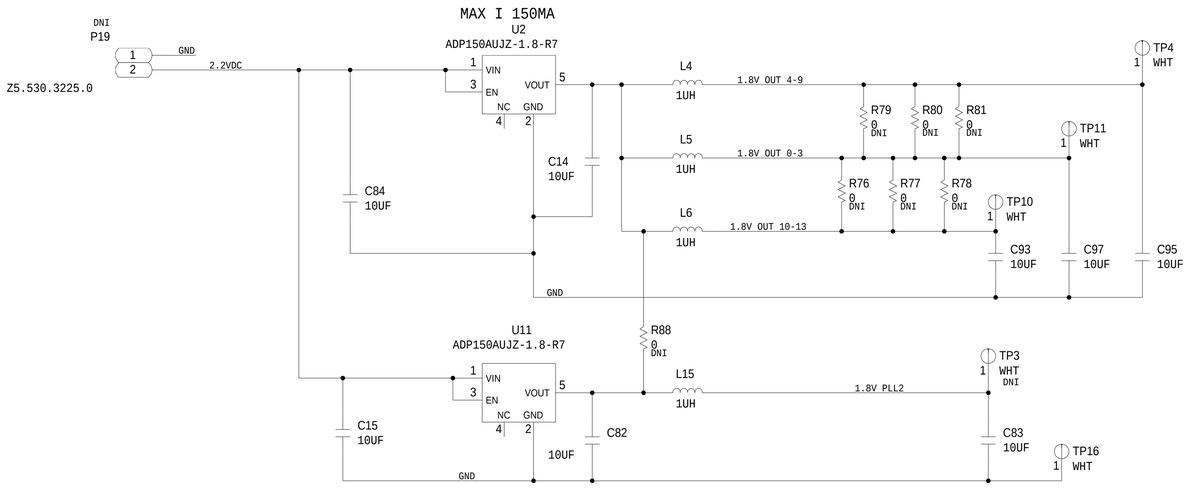
	PTD ENGINEER R.Huntley	SIZE D	SCALE NONE
		SHEET 3 OF 5	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

3.3V REGULATORS



1.8V REGULATOR



ANALOG DEVICES	SCHEMATIC		
	<DRAWING_TITLE_HEADER> AD9523 EVALUATION BOARD		
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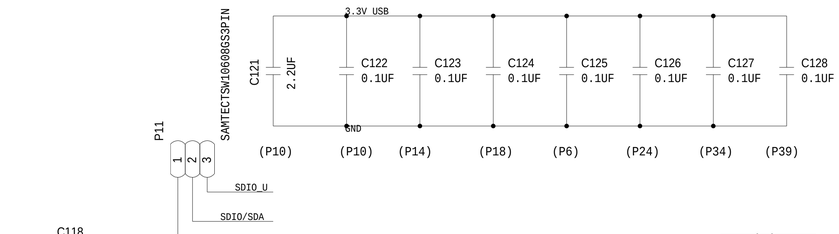
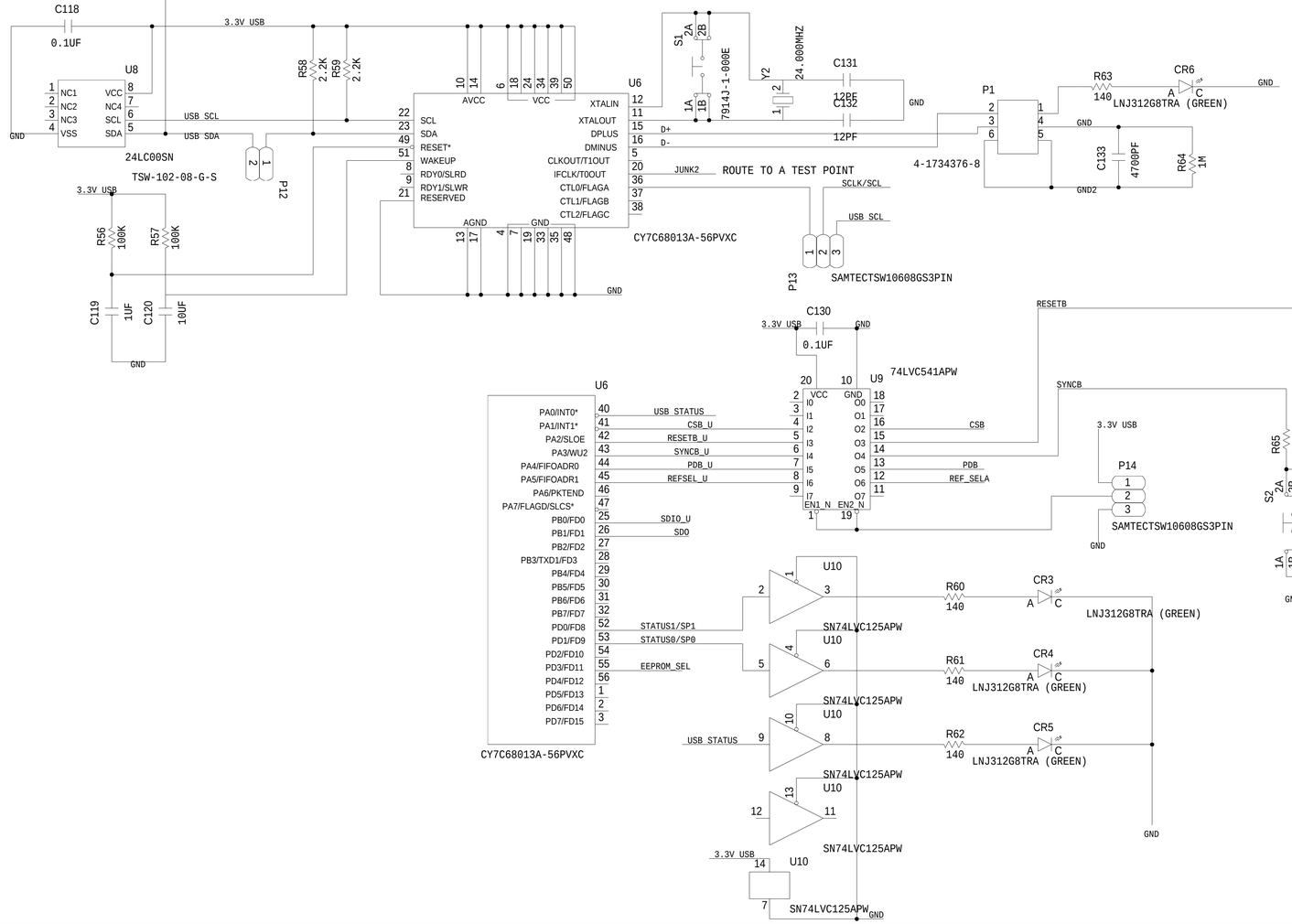
	PTD ENGINEER R.Huntley	SIZE D	SCALE NONE
		SHEET 4 OF 5	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

USB INTERFACE

BYPASS CAPS FOR CY7C68013A





ANALOG DEVICES

SCHEMATIC

<DRAWING_TITLE_HEADER>
AD9523
EVALUATION BOARD

DESIGN VIEW
<DESIGN_VIEW>

DRAWING NO.
9523EE01

REV
E

PTD ENGINEER
R.Huntley

SIZE
D

SCALE
NONE

SHEET 5 OF 5